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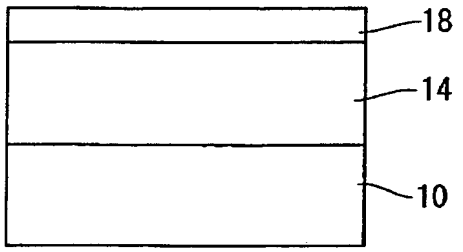
最終頁に続く

(54)【発明の名称】　半導体基板の製造方法

(57)【要約】
【課題】厚い応力緩和された平滑なＳｉＧｅ層を形成する。
【解決手段】　比較的高いＧｅ濃度を有するＳｉＧｅ層を形成する方法を包含する半導体基板の製造方法であって、シリコン基板を提供する工程と、Ｇｅ濃度がモル分率で２２％以上であるＳｉＧｅ層を約１００ｎｍ～５００ｎｍの厚さに堆積する工程と、約１・10^{16} ｃｍ$^{-2}$～５・10^{16} ｃｍ$^{-2}$のドーズ量で、約２０ｋｅＶ～４０ｋｅＶのエネルギで、H^+ イオンをＳｉＧｅ層に注入する工程と、不活性雰囲気中で、約６５０℃～９５０℃の温度で、約３０秒～３０分間、シリコン基板およびＳｉＧｅ層を熱アニーリングして、ＳｉＧｅ層を緩和する工程と、緩和ＳｉＧｅ層上に、引張歪みのかかったシリコンの層を約５ｎｍ～３０ｎｍの厚さに堆積する工程とを含む。



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【特許請求の範囲】

【請求項１】　比較的高いＧｅ濃度を有するＳｉＧｅ層を形成する方法を包含する半導体基板の製造方法であって、

シリコン基板を提供する工程と、

Ｇｅ濃度がモル分率で２２％以上であるＳｉＧｅ層を約１００ｎｍ～５００ｎｍの厚さに堆積する工程と、

約１・１０^{16} ｃｍ$^{-2}$～５・１０^{16} ｃｍ$^{-2}$ のドーズ量で、約２０ｋｅＶ～４０ｋｅＶのエネルギで、H^+ イオンを該ＳｉＧｅ層に注入する工程と、

不活性雰囲気中で、約６５０℃～９５０℃の温度で、約３０秒～３０分間、該シリコン基板および該ＳｉＧｅ層を熱アニーリングして、該ＳｉＧｅ層を緩和する工程と、

該緩和ＳｉＧｅ層上に、引張歪みのかかったシリコン層を約５ｎｍ～３０ｎｍの厚さに堆積する工程と、を含む、半導体基板の製造方法。

【請求項２】　前記ＳｉＧｅの層を堆積する工程が、約４００℃～６００℃の温度で該ＳｉＧｅの層を堆積する、請求項１に記載の方法。

【請求項３】　前記注入工程よりも前に、前記ＳｉＧｅ層上にシリコン酸化物の層を約５０Å～３００Åの厚さに堆積する工程をさらに含む、請求項１に記載の方法。

【請求項４】　前記熱アニーリング工程よりも後に、前記緩和ＳｉＧｅ層上に約１００ｎｍの厚さを有する緩和ＳｉＧｅの層を堆積する工程をさらに含む、請求項１に記載の方法。

【請求項５】　前記熱アニーリング工程は、アルゴン雰囲気中で行われる、請求項１に記載の方法。

【請求項６】　比較的高いＧｅ濃度を有するＳｉＧｅ層を形成する方法を包含する半導体基板の製造方法であって、

バルクシリコンおよびＳＩＭＯＸからなる基板のいずれかより選択されたシリコン基板を提供する工程と、

Ｇｅ濃度がモル分率で２５％以上のＳｉＧｅ層を、約４００℃～６００℃の範囲内の温度で、約１００ｎｍ～５００ｎｍの厚さに堆積する工程と、

約１・１０^{16} ｃｍ$^{-2}$～５・１０^{16} ｃｍ$^{-2}$ のドーズ量で、約２０ｋｅＶ～４５ｋｅＶのエネルギで、H^+ イオンを該ＳｉＧｅ層に注入する工程と、

アルゴン雰囲気中で、約６５０℃～９５０℃の温度で、約３０秒～３０分間、該シリコン基板および該ＳｉＧｅ層を熱アニーリングして、該ＳｉＧｅ層を緩和する工程と、

該緩和ＳｉＧｅ層上に、引張歪みのかかったシリコンの層を約５ｎｍ～３０ｎｍの厚さに堆積する工程と、を含む、半導体基板の製造方法。

【請求項７】　前記注入工程よりも前に、前記ＳｉＧｅ層上にシリコン酸化物の層を約５０Å～３００Åの厚さに堆積する工程をさらに含む、請求項６に記載の方法。

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【請求項８】　前記緩和ＳｉＧｅ層の厚さが３００ｎｍ未満である場合に、前記熱アニーリング工程よりも後に、前記緩和ＳｉＧｅ層上に約１００ｎｍの厚さを有する緩和ＳｉＧｅの層を堆積する工程をさらに含む、請求項６に記載の方法。

【請求項９】　比較的高いＧｅ濃度を有するＳｉＧｅ層を形成する方法を包含する半導体基板の製造方法であって、

シリコン基板を提供する工程と、

約４００℃～６００℃の範囲内の温度で、Ｇｅ濃度がモル分率で２２％以上のＳｉＧｅ層を約１００ｎｍ～５００ｎｍの厚さに堆積する工程と、

約１・１０^{16} ｃｍ$^{-2}$～５・１０^{16} ｃｍ$^{-2}$ のドーズ量で、約２０ｋｅＶ～４５ｋｅＶのエネルギで、H^+ イオンを該ＳｉＧｅ層に注入する工程と、

不活性雰囲気中で、約６５０℃～９５０℃の温度で、約３０秒～３０分間、該シリコン基板および該ＳｉＧｅ層を熱アニーリングして、少なくとも７０％の緩和が達成されるように該ＳｉＧｅ層を緩和する工程と、

該緩和ＳｉＧｅ層上に、引張歪みのかかったシリコンの層を約５ｎｍ～３０ｎｍの厚さに堆積する工程と、を含む、半導体基板の製造方法。

【請求項１０】　前記注入工程よりも前に、前記ＳｉＧｅ層上にシリコン酸化物の層を約５０Å～３００Åの厚さに堆積する工程をさらに含む、請求項９に記載の方法。

【請求項１１】　前記熱アニーリング工程は、アルゴン雰囲気中で行われる、請求項９に記載の方法。

【請求項１２】　前記熱アニーリング工程よりも後に、前記緩和ＳｉＧｅ層上に約１００ｎｍの厚さを有する緩和ＳｉＧｅの層を堆積する工程をさらに含む、請求項９に記載の方法。

【請求項１３】　前記緩和ＳｉＧｅ層の厚さが３００ｎｍ未満である場合にのみ、前記緩和ＳｉＧｅ層上に約１００ｎｍの厚さを有する緩和ＳｉＧｅの層を堆積する工程が行われる、請求項１２に記載の方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】（関連出願）本出願は、２０００年４月３日に出願された米国特許出願第０９／５４１，２５５号の「Ｓｉ上に厚い緩和ＳｉＧｅ層を形成する方法」、ならびに２００１年２月１３日に出願された米国特許出願第０９／７８３，８１７号の「$Si_{1-x}Ge_x$ ＣＭＯＳの漏れ電流を低減する方法」に関連する。

(発明の領域）本発明は、高速ＣＭＯＳ集積回路等の半導体基板の製造方法に関し、詳細には、水素注入を用いてＳｉＧｅ層を形成する工程を包含する半導体基板の製造方法に関する。

【０００２】

【従来の技術】移動度の向上したＭＯＳＦＥＴデバイスアプリケーションにおいて、キャリア移動度を向上させるために、ｎＭＯＳデバイス（Ｗｅｌｓｅｒらの”Ｓｔｒａｉｎ ｄｅｐｅｎｄｅｎｃｅ ｏｆ ｔｈｅ ｐｅｒｆｏｒｍａｎｃｅ ｅｎｈａｎｃｅｍｅｎｔ ｉｎ ｓｔｒａｉｎｅｄ－Ｓｉ ｎ－ＭＯＳＦＥＴｓ”，ＩＥＤＭ Ｃｏｎｆｅｒｅｎｃｅ Ｐｒｏｃｅｅｄｉｎｇｓ，ｐ．３７３（１９９４）（非特許文献１）、Ｒｉｍらの”Ｆａｂｒｉｃａｔｉｏｎ ａｎｄａｎａｌｙｓｉｓ ｏｆ Ｄｅｅｐ ｓｕｂｍｉｃｒｏｎ ｓｔｒａｉｎｅｄ－Ｓｉ Ｎ－ＭＯＳＦＥＴｓ”，ＩＥＥＥ Ｔｒａｎｓａｃｔｉｏｎｓ ｏｎＥｌｅｃｔｒｏｎ Ｄｅｖｉｃｅｓ，Ｖｏｌ４７，１４０６，（２０００）（非特許文献２）、およびＲｉｍらの”Ｓｔｒａｉｎｅｄ Ｓｉ ＮＭＯＳＦＥＴｓ ｆｏｒ ｈｉｇｈ ｐｅｒｆｏｒｍａｎｃｅ ＣＭＯＳ ｔｅｃｈｎｏｌｏｇｙ，２００１ Ｓｙｍｐｏｓｉｕｍ ｏｎ ＶＬＳＩ Ｔｅｃｈｎｏｌｏｇｙ Ｄｉｇｅｓｔ ｏｆ Ｔｅｃｈｎｉｃａｌ Ｐａｐｅｒｓ，ｐ．５９，ＩＥＥＥ ２００１（非特許文献３））ならびにｐＭＯＳデバイス（Ｒｉｍらの”Ｅｎｈａｎｃｅｄ ｈｏｌｅ ｍｏｂｉｌｉｔｉｅｓ ｉｎ ｓｕｒｆａｃｅ－ｃｈａｎｎｅｌ ｓｔｒａｉｎｅｄ－Ｓｉ ｐ－ＭＯＳＦＥＴｓ”，ＩＥＤＭ Ｃｏｎｆｅｒｅｎｃｅ Ｐｒｏｃｅｅｄｉｎｇｓ，ｐ．５１７（１９９５）（非特許文献４）、およびＮａｙａｋらの”Ｈｉｇｈ－ｍｏｂｉｌｉｔｙＳｔｒａｉｎｅｄ－Ｓｉ ＰＭＯＳＦＥＴｓ”，ＩＥＥＥ Ｔｒａｎｓａｃｔｉｏｎｓ ｏｎ Ｅｌｅｃｔｒｏｎ Ｄｅｖｉｃｅｓ，Ｖｏｌ．４３，１７０９（１９９６）（非特許文献５））の両方について、厚い応力緩和された$Si_{1-x}Ge_x$バッファ層を、薄い歪シリコン層のための仮想基板として用いられている。バルクシリコンデバイスと比較して、Ｌｅｆｆ＜７０ｎｍであるデバイスにおいて、電子移動度が７０％向上したことがＲｉｍらの２００１年の文献に報告されている。長チャネルデバイスにおける高電界ホール移動度(high-field hole mobilityが４０％まで向上したことが、Ｎａｙａｋらによって報告されている。

【０００３】厚い$Si_{1-x}Ge_x$層は、ミスフィット転位の形成により可塑的に、歪み（応力）が緩和する（Ｒ．Ｈｕｌｌらの”Ｎｕｃｌｅａｔｉｏｎ ｏｆ ｍｉｓｆｉｔ ｄｉｓｌｏｃａｔｉｏｎｓ ｉｎ ｓｔｒａｉｎｅｄ－ｌａｙｅｒ ｅｐｉｔａｘｙ ｉｎ ｔｈｅ Ge_xSi_{1-x}／Ｓｉ ｓｙｓｔｅｍ”，Ｊ．Ｖａｃ Ｓｃｉ．Ｔｅｃｈｎｏｌ．，Ａ７，２５８０，１９８９（非特許文献６）、Ｈｏｕｇｈｔｏｎの”Ｓｔｒａｉｎ ｒｅｌａｘａｔｉｏｎｋｉｎｅｔｉｃｓ ｉｎ $Si_{1-x}Ge_x$／Ｓｉ ｈｅｔｅｒｏｓｔｒｕｃｔｕｒｅｓ”，Ｊ．Ａｐｐｌ．Ｐｈｙｓ．，７０，２１３６，１９９１（非特許文献７）、Ｗｉｃｋｅｎｈａｕｓｅｒらの”Ｄｅｔｅｒｍｉｎａｔｉｏｎ ｏｆ ｔｈｅ ａｃｔｉｖａｔｉｏｎ ｅｎｅｒｇｙ ｆｏｒ ｔｈｅｈｅｔｅｒｏｇｅｎｅｏｕｓ ｎｕｃｌｅａｔｉｏｎ ｏｆ ｍｉｓｆｉｔ ｄｉｓｌｏｃａｔｉｏｎｓ ｉｎ $Si_{1-x}Ge_x$／Ｓｉ ｄｅｐｏｓｉｔｅｄｂｙ ｓｅｌｅｃｔｉｖｅ ｅｐｉｔａｘｙ”，Ａｐｐｌ．Ｐｈｙｓ．Ｌｅｔｔ．，７０，３２４，１９９７（非特許文献８）、Ｍａｔｔｈｅｗｓらの”Ｄｅｆｅｃｔｓ ｉｎ ｅｐｉｔａｘｉａｌ ｍｕｌｔｉｌａｙｅｒｓ”，Ｊ．Ｃｒｙｓｔ．Ｇｒｏｗｔｈ，２７，１１８，１９７４（非特許文献９）、およびＴａｎｇらの”Ｉｎｖｅｓｔｉｇａｔｉｏｎ ｏｆ ｄｉｓｌｏｃａｔｉｏｎｓ ｉｎ $Si_{1-x}Ge_x$／Ｓｉ ｈｅｔｅｒｏｓｔｒｕｃｔｕｒｅｓ ｇｒｏｗｎ ｂｙ ＬＰＣＶＤ”，Ｊ．Ｃｒｙｓｔ．Ｇｒｏｗｔｈ，１２５，３０１，１９９２（非特許文献１０））。

【０００４】しかし、このプロセスの間、通常、貫通転位が発生する。貫通転位の存在によりデバイスの性能が低下し、デバイスの歩留まりが著しく低下する。

【０００５】高品質の歪み緩和$Si_{1-x}Ge_x$バッファ層を製造する現在の最新技術は、組成の割合が厚さ方向に異なる（傾斜された）数μｍの厚さを有する層の成長である（Ｒｉｍらによる２０００年の上記文献、Ｎａｙａｋらの上記文献、Ｓｃｈａｅｆｆｌｅｒらの”Ｈｉｇｈ－ｅｌｅｃｔｒｏｎ－ｍｏｂｉｌｉｔｙ Ｓｉ／ＳｉＧｅ ｈｅｔｅｒｏｓｔｒｕｃｔｕｒｅｓ：ｉｎｆｌｕｅｎｃｅ ｏｆｔｈｅ ｒｅｌａｘｅｄ ＳｉＧｅ ｂｕｆｆｅｒ ｌａｙｅｒ”，Ｓｅｍｉｃｏｎｄｕｃｔｏｒ．Ｓｃｉ．Ｔｅｃｈｎｏｌ．，７．２６０，１９９２（非特許文献１１）、およびＦｉｔｚｇｅｒａｌｄらの”Ｔｏｔａｌｌｙ ｒｅｌａｘｅｄ Ge_xSi_{1-x} ｌａｙｅｒｓ ｗｉｔｈ ｌｏｗ ｔｈｒｅａｄｉｎｇ ｄｉｓｌｏｃａｔｉｏｎ ｄｅｎｓｉｔｉｅｓ ｇｒｏｗｎ ｏｎＳｉ ｓｕｂｓｔｒａｔｅｓ”，Ａｐｐｌ．Ｐｈｙｓ．Ｌｅｔｔ．，５９，８１１，１９９１（非特許文献１２））。しかし、貫通転位の密度は依然として高く、例えば典型的には$10E6cm^{-2}$を超える。さらに、数μｍの厚さを有する$Si_{1-x}Ge_x$層を市販の実用可能なデバイスの製造に組み込むことは、現実的ではない。ＳＩＭＯＸ（Ｓｅｐａｒａｔｉｏｎ ｂｙ Ｉｍｐｌａｎｔａｔｉｏｎ ｏｆ Ｏｘｙｇｅｎ）ウエハ上におけるＳｉＧｅ成長の緩和についてもまた研究が行われており、この場合、Ｓｉ／ＳｉＧｅ二重層は、基板によって平坦に維持されたフリーフローティングフォイル(free-floating foil)として振る舞う。しかし、シリコンとＳｉＧｅ層との厚さの比は、ＳｉＧｅ層からシリコン層への転位の核形成および転位のすべりが起こるように正確に制御されねばならない。また、この技術は、ほとんどの技術アプ

リケーションに使用できるようにするため、より多量のゲルマニウムを含有するように展開される必要がある（LeGouseらの"Relaxation of SiGe thin films grown on Si／SiO_2 substrates", J. Appl. Phys. 75（11） 1994（非特許文献１３）、およびPowellらの"New approach to the growth of low dislocation relaxed SiGe material", Appl. Phys. Lett., vol. 64, 1856（1994）（非特許文献１４））。

【０００６】ヘリウム注入およびアニーリングによってシリコンおよびＧｅならびにそれらの合金内に形成された孔は、転位との間に強力で短距離の相互誘引作用を有することがわかっている。ＳｉＧｅ／Ｓｉ界面に孔を設けることによって、応力緩和率が大幅に向上され、転位微細構造が変形される。しかし、貫通転位密度の低減は観察されなかった（Follstaedtらの"Cavity-dislocation interactions in Si-Ge and implications for heterostructure relaxation", Appl. Phys. Lett., 69, 2059, 1996（非特許文献１５））。８０%の緩和を達成するためには、依然、アニーリングを約１０００℃で１時間行う必要がある。

【０００７】また、水素注入により、シリコンの剥離が引き起こされ、シリコンで形成された微細層の剪断が発生することがわかっている（Weldonらの"On the mechanism of the hydrogen-inducedexfoliation of silicon", J. Vac. Sci. Technol. B. 15, 1065, 1997（非特許文献１６））。この技術は、高品質ＳＯＩ（silicon-on-insulator）ウエハの製造に用いられており、「SmartCut」（商標）プロセスとして公知である。ドイツの共同研究による最近の文献（S. Mantlらの文献およびH. Trinkausらの文献）は、水素注入を用いてＳｉＧｅの緩和度を上昇させ、貫通転位の密度を低減することの利点を報告している。（S. Mantlらの"Strain relaxation of epitaxial SiGe layers on Si（100） improved by hydrogen implantation, Nuclear Instruments and Methods in Physics ResearchB 147, 29, （1999）（非特許文献１７）、およびH. Trinkausらの"Strain relaxation mechanismfor hydrogen-implanted $Si_{1-x}Ge_x$／Si（100） heterostructures", Appl. Phys. Lett., 76, 3552, 2000（非特許文献１８））しかし、上記研究者らは、厚さがわずか２０００Å～２５００Åであり、Ｇｅ濃度がモル重量で２２%未満であるＳｉＧｅ層の緩和を報告している。このような厚さを有するＳｉＧｅ層は、市販のデバイスアプリケーションにとって十分ではない。より厚い膜を形成する方法が、関連出願である米国特許出願第０９／５４１，２５５号に開示されており、適切な絶縁によって漏れ電流を低減する方法が、関連出願である米国特許出願第０９／７８３，８１７号に開示されている。関連米国特許出願第０９／５４１，２５５号は、約２１%のＧｅを含むＳｉＧｅ薄膜の形成について記載している。キャップシリコンチャネル内の歪みを増大し、電子移動度およびホール移動度をさらに向上させるために、Ｇｅ濃度をより高くするのが望ましい。

【０００８】ドイツの共同研究は、３０%までのＧｅを含有する大幅に緩和されたＳｉＧｅ層を形成する際に、ヘリウム注入が有効であると報告している（M. Luysbergらの"Relaxation of $Si_{1-x}Ge_x$ bufferlayers on Si（100） through Helium implantation", Abstracts of the 2001 MRS Spring Meeting, Abstract P5. 4, April 18, 2001（非特許文献１９））。

【０００９】

【非特許文献１】Welserらの"Strain dependence of the performance enhancement in strained-Si n-MOSFETs", IEDM Conference Proceedings, p. 373, 1994、

【非特許文献２】Rimらの"Fabrication and analysis of Deep submicron strained-Si N-MOSFETs", IEEE Transactions on Electron Devices, Vol47, 1406, 2000

【非特許文献３】Rimらの"Strained Si NMOSFETs for highperformance CMOS technology, 2001 Symposium on VLSI Technology Digest of Technical Papers, p. 59, IEEE 2001

【非特許文献４】pMOSデバイス（Rimらの"Enhanced hole mobilities in surface-channel strained-Sip-MOSFETs", IEDM Confe

rence Proceedings, p. 517, 1995.
【非特許文献5】Nayakらの"High-mobility Strained-Si PMOSFETs", IEEE Transactions on Electron Devices, Vol. 43, 1709 (1996)
【非特許文献6】R. Hullらの"Nucleation of misfit dislocations in strained-layer epitaxy inthe Ge_xSi_{1-x}/Si system", J. Vac Sci. Technol., A7, 2580, 1989.
【非特許文献7】Houghtonの"Strain relaxation kinetics in $Si_{1-x}Ge_x$/Si heterostructures", J. Appl. Phys., 70, 2136, 1991.
【非特許文献8】Wickenhauserらの"Determination of theactivation energy for the heterogeneous nucleation of misfit dislocations in $Si_{1-x}Ge_x$/Si deposited by selective epitaxy", Appl. Phys. Lett., 70, 324, 1997.
【非特許文献9】Matthewsらの"Defects in epitaxial multilayers", J. Cryst. Growth, 27, 118, 1974.
【非特許文献10】Tangらの"Investigation of dislocations in $Si_{1-x}Ge_x$/Si heterostructures grown by LPCVD", J. Cryst. Growth, 125, 301, 1992
【非特許文献11】Schaefflerらの"High-electron-mobilitySi/SiGe heterostructures: influenceof the relaxed SiGe buffer layer", Semiconductor. Sci. Technol., 7. 260, 1992
【非特許文献12】Fitzgeraldらの"Totally relaxed Ge_xSi_{1-x} layers with low threading dislocation densities grown on Si substrates", Appl. Phys. Lett., 59, 811, 1991
【非特許文献13】LeGouseらの"Relaxation of SiGe thin films grown on Si/SiO_2 substrates", J. Appl. Phys. 75(11), 1994
【非特許文献14】Powellらの"New approach to the growthof low dislocation relaxed SiGe material", Appl. Phys. Lett., vol. 64, 1856, 1994
【非特許文献15】Follstaedtらの"Cavity-dislocation interactions in Si-Ge and implicationsfor heterostructure relaxation", Appl. Phys. Lett., 69, 2059, 1996
【非特許文献16】Weldonらの"On the mechanism of the hydrogen-induced exfoliation of silicon", J. Vac. Sci. Technol. B. 15, 1065, 1997
【非特許文献17】S. Mantlらの"Strain relaxation of epitaxial SiGe layers on Si(100) improved by hydrogen implantation, NuclearInstruments and Methods in Physics Research B 147, 29, 1999
【非特許文献18】H. Trinkausらの"Strain relaxation mechanism for hydrogen-implanted $Si_{1-x}Ge_x$/Si(100) heterostructures", Appl. Phys. Lett., 76, 3552, 2000
【非特許文献19】M. Luysbergらの"Relaxation of $Si_{1-x}Ge_x$ buffer layers on Si(100) through Helium implantation", Abstracts of the 2001 MRS Spring Meeting, AbstractP5.4, April 18, 2001

【0010】

【発明が解決しようとする課題】この論文の口頭発表において、$1\cdot10^{16}\ cm^{-2}$～$3\cdot10^{16}\ cm^{-2}$のドーズ量で18keVヘリウムイオンが注入され、750℃～1000℃のRTA処理が施された30%のGe濃度を有する100nmの厚さのSiGe層において、80%の応力緩和が達成されたことが具体的に報告されている。発表者は、Ge濃度が22%よりも高い場合、水素注入は有効ではないと具体的に述べている。2

２％を超えるＧｅ濃度を有する平滑な１００ｎｍ～５００ｎｍの厚さの応力緩和ＳｉＧｅ層を形成するために、ヘリウム注入が必要であり、水素注入は有効でないことが報告されている。

【００１１】本発明の目的は、水素注入を用いて、高いＧｅ濃度（２２％以上、モル分率）を有する厚い（例えば１００ｎｍ～５００ｎｍ）応力緩和された平滑なＳｉＧｅ層（膜）を、高速ＭＯＳＦＥＴアプリケーションのために用いられる引張歪みのかかったシリコン膜のためのバッファ層として形成することである。

【００１２】

【課題を解決するための手段】本発明の半導体基板の製造方法は、比較的高いＧｅ濃度を有するＳｉＧｅ層を形成する方法を包含する半導体基板の製造方法であって、シリコン基板を提供する工程と、Ｇｅ濃度がモル分率で２２％以上であるＳｉＧｅ層を約１００ｎｍ～５００ｎｍの厚さに堆積する工程と、約$1\cdot10^{16}$ cm^{-2}～$5\cdot10^{16}$ cm^{-2}のドーズ量で、約２０ｋｅＶ～４０ｋｅＶのエネルギで、H^+イオンを該ＳｉＧｅ層に注入する工程と、不活性雰囲気中で、約６５０℃～９５０℃の温度で、約３０秒～３０分間、該シリコン基板および該ＳｉＧｅ層を熱アニーリングして、該ＳｉＧｅ層を緩和する工程と、該緩和ＳｉＧｅ層上に、引張歪みのかかったシリコン層を約５ｎｍ～３０ｎｍの厚さに堆積する工程とを含む。

【００１３】前記ＳｉＧｅの層を堆積する工程が、約４００℃～６００℃の温度で該ＳｉＧｅの層を堆積する。

【００１４】前記注入工程よりも前に、前記ＳｉＧｅ層上にシリコン酸化物の層を約５０Å～３００Åの厚さに堆積する工程をさらに含む。

【００１５】前記熱アニーリング工程よりも後に、前記緩和ＳｉＧｅ層上に約１００ｎｍの厚さを有する緩和ＳｉＧｅの層を堆積する工程をさらに含む。

【００１６】前記熱アニーリング工程は、アルゴン雰囲気中で行われる。

【００１７】また、本発明の半導体基板の製造方法は、比較的高いＧｅ濃度を有するＳｉＧｅ層を形成する方法を包含する半導体基板の製造方法であって、バルクシリコンおよびＳＩＭＯＸからなる基板のいずれかより選択されたシリコン基板を提供する工程と、Ｇｅ濃度がモル重量で２５％以上のＳｉＧｅ層を、約４００℃～６００℃の範囲内の温度で、約１００ｎｍ～５００ｎｍの厚さに堆積する工程と、約$1\cdot10^{16}$ cm^{-2}～$5\cdot10^{16}$ cm^{-2}のドーズ量で、約２０ｋｅＶ～４５ｋｅＶのエネルギで、H^+イオンを該ＳｉＧｅ層に注入する工程と、アルゴン雰囲気中で、約６５０℃～９５０℃の温度で、約３０秒～３０分間、該シリコン基板および該ＳｉＧｅ層を熱アニーリングして、該ＳｉＧｅ層を緩和する工程と、該緩和ＳｉＧｅ層上に、引張歪みのかかったシリコン層を約５ｎｍ～３０ｎｍの厚さに堆積する工程とを含む。

【００１８】前記注入工程よりも前に、前記ＳｉＧｅ層上にシリコン酸化物の層を約５０Å～３００Åの厚さに堆積する工程をさらに含む。

【００１９】前記緩和ＳｉＧｅ層の厚さが３００ｎｍ未満である場合に、前記熱アニーリング工程よりも後に、前記緩和ＳｉＧｅ層上に約１００ｎｍの厚さを有する緩和ＳｉＧｅの層を堆積する工程をさらに含む。

【００２０】また、本発明の半導体基板の製造方法は、比較的高いＧｅ濃度を有するＳｉＧｅ層を形成する方法を包含する半導体基板の製造方法であって、シリコン基板を提供する工程と、約４００℃～６００℃の範囲内の温度で、Ｇｅ濃度がモル分率で２２％以上のＳｉＧｅ層を約１００ｎｍ～５００ｎｍの厚さに堆積する工程と、約$1\cdot10^{16}$ cm^{-2}～$5\cdot10^{16}$ cm^{-2}のドーズ量で、約２０ｋｅＶ～４５ｋｅＶのエネルギで、H^+イオンを該ＳｉＧｅ層に注入する工程と、不活性雰囲気中で、約６５０℃～９５０℃の温度で、約３０秒～３０分間、該シリコン基板および該ＳｉＧｅ層を熱アニーリングして、少なくとも７０％の緩和が達成されるように該ＳｉＧｅ層を緩和する工程と、該緩和ＳｉＧｅ層上に、引張歪みのかかったシリコンの層を約５ｎｍ～３０ｎｍの厚さに堆積する工程とを含む。

【００２１】前記注入工程よりも前に、前記ＳｉＧｅ層上にシリコン酸化物の層を約５０Å～３００Åの厚さに堆積する工程をさらに含む。

【００２２】前記熱アニーリング工程は、アルゴン雰囲気中で行われる。

【００２３】前記熱アニーリング工程よりも後に、前記緩和ＳｉＧｅ層上に約１００ｎｍの厚さを有する緩和ＳｉＧｅの層を堆積する工程をさらに含む。

【００２４】前記緩和ＳｉＧｅ層の厚さが３００ｎｍ未満である場合にのみ、前記緩和ＳｉＧｅ層上に約１００ｎｍの厚さを有する緩和ＳｉＧｅの層を堆積する工程が行われる。

【００２５】上記した本発明の目的および要旨は、本発明の本質を素早く理解できるように提供されたものである。以下に図面と関連付けて説明する本発明の好適な実施形態の詳細な説明を参照することにより、本発明をより完全に理解し得る。

【００２６】

【発明の実施の形態】本明細書の開示は、従来技術による教示とは逆に、２２％以上のＧｅ濃度を有する大幅に歪み（応力）緩和されたＳｉＧｅ膜を形成する際に、水素注入が非常に有用であることを示す。本明細書に記載の技術を、モル重量比で２２％を超えるＧｅ濃度を有するＳｉＧｅ層（膜）に適用するが、本発明の方法を用いる場合、Ｇｅ濃度の上限は指示されない。ヘリウムは、欠陥を不動態化できないが、水素は欠陥を不動態化できることがよく知られているので、市販のデバイスアプリ

ケーションの場合、ヘリウムよりも水素注入の方が好ましい。本発明の方法は、水素注入を用いて、高いＧｅ濃度（モル分率で２２％以上）を有し、且つ、低い貫通転位密度を有する厚い（例えば１００ｎｍ～５００ｎｍ）応力緩和された平滑なＳｉＧｅ層（膜）を形成する。

【００２７】本発明の方法を、まず図１を参照して説明する。初めに、シリコン基板１０が提供される。シリコン基板１０は、バルクシリコンまたはＳＩＭＯＸ（Ｓｅｐａｒａｔｉｏｎ　ｂｙ　Ｉｍｐｌａｎｔａｔｉｏｎ　ｏｆ　Ｏｘｙｇｅｎ）であり得る。シリコン基板１０上に、歪ＳｉＧｅ層１２が約１００～５００ｎｍの厚さに堆積される。歪ＳｉＧｅ層１２のＧｅ濃度は、原子比率（モル分率）で２２％以上であり得る。本発明の方法の好適な実施形態では、約３０％のＧｅ濃度を有するＳｉＧｅ層１２を形成する。あるいは、傾斜されたＧｅプロフィール、すなわち、厚さ方向におけるＧｅ濃度が、厚くなるほど高くなっているＳｉＧｅ層１２が使用され得る。成長条件および材料ガスは、良好な結晶性を確保すると共に、表面の凹凸が最小化されるように選択する必要がある。このことは、通常、例えば４００℃～６００℃での低温成長を行って、準安定歪ＳｉＧｅ膜を形成することを意味する。

【００２８】図２を参照すると、H^+ イオンが注入される。H^+ のドーズ量は約$1 \cdot 10^{16}$ cm^{-2}～$5 \cdot 10^{16}$ cm^{-2}の範囲内である。エネルギレベルは、ＳｉＧｅの厚さに依存するが、通常、約２０ｋｅＶ～４５ｋｅＶの範囲内である。注入工程が実施される間の汚染を避けるために、約５０Å～３００Å（５～３０ｎｍ）の薄い犠牲シリコン酸化物層(sacrificial silicon oxide layer)をＳｉＧｅ層１２上に堆積してもよい。

【００２９】図３は、熱アニーリング工程を示す。この熱アニーリングにより、歪ＳｉＧｅ層１２が第１の歪み（応力）緩和ＳｉＧｅ層１４に変化する。アニーリングは、Ａｒ等の不活性雰囲気内において、約６５０℃～９５０℃の範囲内の温度で約３０秒から３０分の間にわたって行われる。

【００３０】必要に応じて、任意に、歪み緩和されたＳｉＧｅからなる第２のＳｉＧｅ層１６を、緩和ＳｉＧｅ層１４上に約１００ｎｍ以上の厚さに堆積する。この任意に設ける層が必要かどうかを判断する基準は、緩和ＳｉＧｅ層１４の厚さである。ＳｉＧｅ層１４が３００ｎｍよりも薄い場合、最終的なＳｉＧｅ緩和層全体の厚さが少なくとも３００ｎｍになるように、追加の歪み緩和ＳｉＧｅ層１６を設けることが要求される。

【００３１】図５に示す本発明の方法の最終工程において、引張応力のかかったシリコン層１８が、約５ｎｍ～３０ｎｍの厚さを有するように、緩和ＳｉＧｅ層１４または第２のＳｉＧｅ層１６上に堆積される。

【００３２】図６、図７、および図８～図１０は、モル重量比で約２５％～３０％のＧｅ濃度を有する２００ｎｍ～２２０ｎｍの厚さのＳｉＧｅ膜の、水素注入および熱緩和後の状態を示す。図６は、Ｇｅ濃度が約２８～３０％であり、２００ｎｍ～２２０ｎｍの厚さを有するＳｉＧｅ層の、水素注入および熱緩和を行った後のノマルスキー顕微鏡画像を示す図である。図７は、図６に示すＳｉＧｅ層のＸ線回折を示す図である。また、図８は、厚さ方向の組成割合が変化した傾斜のあるＧｅプロフィールを有する厚さ３００ｎｍのＳｉＧｅ膜の、水素注入およびアニーリングを行った後の４００倍のノマルスキー顕微鏡画像を示す図、図９は、傾斜のあるＧｅプロフィールを有する厚さ３００ｎｍのＳｉＧｅ膜の、水素注入およびアニーリングを行った後の１０００倍のノマルスキー顕微鏡画像を示す図である。図１０は、図８および図９のＳｉＧｅ層のＸ線回折を示す図である。

【００３３】図６、図８および図９のノマルスキー顕微鏡画像は、非常に平坦な表面の状態を示している。図７および図１０は、それぞれ、Ｘ線回折の逆格子空間マップ(reciprocal space map)を示し、これらのマップから、少なくとも７０％から８５％までの結晶格子の大幅な歪み緩和が得られることが確認される。図７を参照すると、この緩和された状態は、破線で示されるように、シリコン（２２４）ピークとＳｉＧｅ（２２４）ピークとの間のオフセットによって示される。

【００３４】図１１は、傾斜のあるＧｅプロフィールを有する約３００ｎｍの厚さを有するＳｉＧｅ膜の、水素注入およびアニーリングを行った後のノマルスキー顕微鏡画像を示す。図１２は、図１１のＳｉＧｅ層のＸ線回折を示す。Ｇｅ濃度は、シリコン基板上の２１％からＳｉＧｅ層表面の３０％へとほぼ直線的に変化する。傾斜のあるＧｅプロフィールを用いることにより、ＳｉＧｅ層の厚さを容易に増加でき、平滑な表面を有する大幅に歪み緩和されたＳｉＧｅ層を提供することもできる。このＳｉＧｅ層は、通常は第２のＳｉＧｅ堆積が必要でなくなるような十分な厚さを有し、それによりＳｉＧｅ層全体の品質が向上する。

【００３５】本発明の方法に基づいて構成された歪み緩和されたＳｉＧｅ層の全てが、引張応力のかかったシリコン膜を成長させるための基板として用いられる。その後、これらの膜を用いて、向上されたホールおよび電子移動度を有するｎＭＯＳおよびｐＭＯＳトランジスタを形成する。図６および図７のＳｉＧｅ薄膜は、２８．６％のＧｅ濃度を有する。ＳｉＧｅ薄層は約２００ｎｍの厚さを有し、約２５ｋｅＶのエネルギで、約$3 \cdot 10^{16}$ cm^{-2}のイオンドーズ量でH^+ イオン注入を行って形成される。ウエハは、ＲＴＡチャンバ内のアルゴン雰囲気中で、約８００℃で約１０分間アニーリングされる。１０００倍のノマルスキー顕微鏡画像は、より平滑な表面を示している。図７のＸ線回折の逆格子空間マップは、大きな中央ピークを示す。このピークは、シリコン（－２－２４）基板ピークである。その下から右にか

けての小さい方のピークは、部分的に緩和されたＳｉＧｅ層から得られたものである。これら２つのピークの相対的な位置から、ＳｉＧｅ層は２８．２%±０．５%のＧｅを有し、７５．８%±３%、応力が緩和されている。

【００３６】図８、図９、および図１０は、約３０%のＧｅ濃度を有する大幅に応力緩和された（例えば約８５%）平滑な第１のＳｉＧｅ層を示す。この例は、ＳｉＧｅ層内のＧｅ濃度が約３０%であり、ＳｉＧｅ層の厚さは約２２０ｎｍである。約２０ｎｍのSiO_2キャップがＰＥＣＶＤによって形成される。H^+イオン注入は、約２６ｋｅＶのエネルギで、約$3\cdot10^{16}\ cm^{-2}$のイオンドーズ量で行われる。ウエハは、ＲＴＡチャンバ内のアルゴン雰囲気中で、約８００℃で９分間アニーリングされる。図９は、ウエハの中央で撮影された４００倍のノマルスキー顕微鏡画像を示す。図９は、同じくウエハの中央で撮影された、同じウエハの１０００倍のノマルスキー画像である。図１０は、そのウエハのＸ線回折を示し、ＳｉＧｅ膜が２９．７%±０．５%のＧｅ濃度を有し、８５．２%±３%、応力緩和されている。

【００３７】図１１および図１２は、大幅に緩和された、平滑な表面を有する傾斜Ｇｅサンプルを示す。図１１は、大幅に緩和された（例えば約８２%）平滑な第１のＳｉＧｅ層のノマルスキー顕微鏡画像であり、ウエハの中心を約１０００倍で撮影したものである。図１２は、図１１のウエハのＸ線回折を示す図である。ＳｉＧｅ層の厚さは約３０１ｎｍであり、成長させたままの状態で約２１%～３０%のＧｅ傾斜プロフィールを有する。H^+イオン注入は、約３２ｋｅＶのエネルギレベルで、約$2\cdot10^{16}\ cm^{-2}$のイオンドーズ量で行われる。ウエハは、ＲＴＡチャンバ内のアルゴン雰囲気中で、約８００℃で９分間アニーリングされる。ＳｉＧｅ層は、２７．８%±０．５%のＧｅ濃度を有し、８２．２%±３%、応力が緩和されている。

（他の実施形態）本発明の方法は、傾斜Ｇｅプロフィールが層の表面において２２%よりも大きなＧｅ濃度を有するように、３００ｎｍを超える厚さのＳｉＧｅ層を成長させ、水素注入（Ｈ－ＩＩ）を行い、ＲＴＡを行って（ＳｉＧｅ層の応力を緩和させ）、それによって引張エピシリコンキャップ／チャネルを形成することによって改変され得る。この実施形態は、第２のＳｉＧｅ層の堆積を必要としない。

【００３８】本発明の方法の他の実施形態は、一定のＧｅプロフィールまたは傾斜のついたＧｅプロフィールを有する第１のＳｉＧｅ層を成長させ、水素注入（Ｈ－ＩＩ）を行い、ＲＴＡを行って（ＳｉＧｅ層の応力を緩和させ）、表面におけるＧｅ濃度が２２%よりも大きな一定のＧｅプロフィールまたは傾斜のついたＧｅプロフィールを有する第２のＳｉＧｅ層を成長させ、それによって引張エピシリコンキャップ／チャネルを形成することを含む。本発明の方法の本実施形態のＳｉＧｅ層の厚さの合計は３００ｎｍ以上である必要がある。

【００３９】以上のように、高Ｇｅ濃度を有する緩和ＳｉＧｅ層を形成する方法を開示した。特許請求の範囲に規定された本発明の範囲内でさらなる変形および修正を行い得ることが理解される。

【００４０】

【発明の効果】本発明の半導体基板の製造方法は、このように、水素注入を用いて、モル分率が２２%以上の高いＧｅ濃度を有する厚い応力緩和された平滑なＳｉＧｅ層を形成することができ、そのＳｉＧｅ層によって、高速ＭＯＳＦＥＴを製造することができる。

【図面の簡単な説明】

【図１】本発明のＳｉＧｅ堆積方法を示す図である。

【図２】本発明のＳｉＧｅ堆積方法を示す図である。

【図３】本発明のＳｉＧｅ堆積方法を示す図である。

【図４】本発明のＳｉＧｅ堆積方法を示す図である。

【図５】本発明のＳｉＧｅ堆積方法を示す図である。

【図６】Ｇｅ濃度が約２８～３０%であり２００ｎｍ～２２０ｎｍの厚さを有するＳｉＧｅ膜の、水素注入および熱緩和を行った後のノマルスキー顕微鏡画像を示す図である。

【図７】図６のウエハのＸ線回折を示す図である。

【図８】傾斜のあるＧｅプロフィールを有する厚さ３００ｎｍのＳｉＧｅ膜の、水素注入およびアニーリングを行った後の４００倍のノマルスキー顕微鏡画像を示す図である。

【図９】傾斜のあるＧｅプロフィールを有する厚さ３００ｎｍのＳｉＧｅ膜の、水素注入およびアニーリングを行った後の１０００倍のノマルスキー顕微鏡画像を示す図である。

【図１０】図８および図９のＳｉＧｅ層のＸ線回折を示す図である。

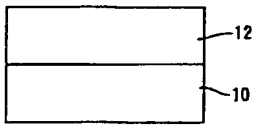
【図１１】傾斜のあるプロフィールを有するように形成された３００ｎｍの厚さのＳｉＧｅ層のノマルスキー顕微鏡画像を示す図である。

【図１２】図１１の３００ｎｍの厚さを有するＳｉＧｅ層の１０００倍のＸ線回折を示す図である。

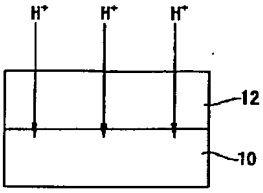
【符号の説明】

１０　シリコン基板
１２　歪ＳｉＧｅ層
１４　緩和ＳｉＧｅ層
１６　第２のＳｉＧｅ層
１８　シリコン層

【図１】

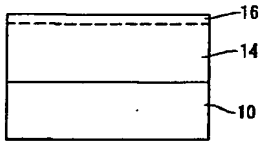


【図２】

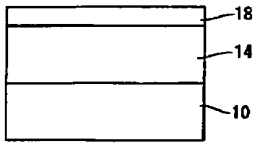


【図３】

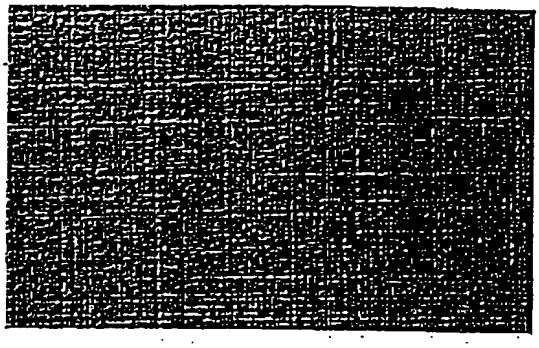
【図４】



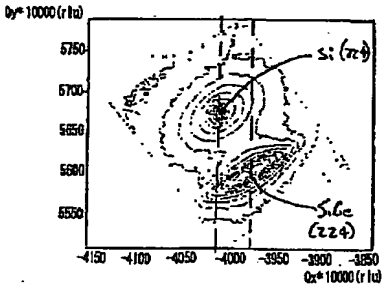
【図５】



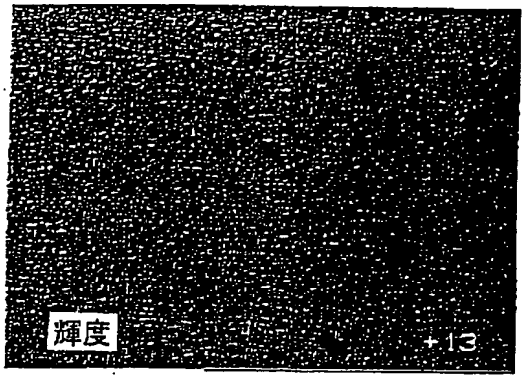
【図６】



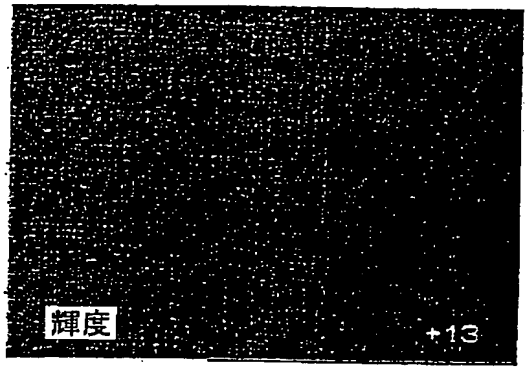
【図７】



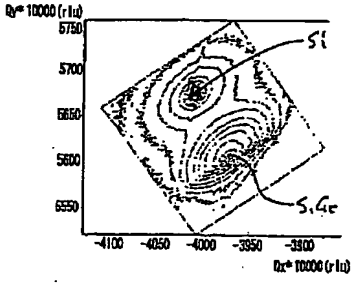
【図８】



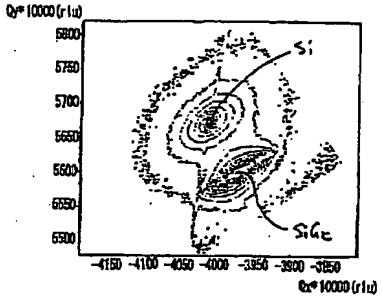
【図９】



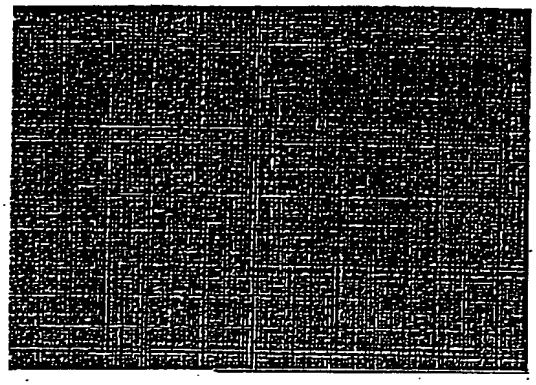
【図１２】



【図１０】



【図１１】



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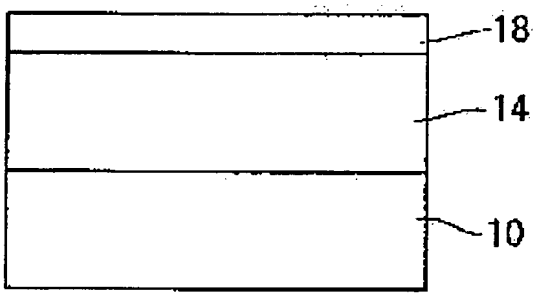
(54) MANUFACTURING METHOD FOR SEMICONDUCTOR SUBSTRATE

(57)Abstract:
PROBLEM TO BE SOLVED: To form a thick and smooth SiGe layer where stress is reduced.
SOLUTION: The method for manufacturing a semiconductor substrate includes a method for forming an SiGe layer having relatively high Ge concentration. It comprises a process to form a silicon substrate, a process where an SiGe layer whose Ge concentration is 22% or higher as mol fraction is deposited to a thickness of 100-500 nm, an H+ ion is implanted in the SiGe layer by a dose amount of 1.1016 cm-2 to 5.1016 cm-2 with an approximate energy of 20-40 keV, a process where the SiGe layer is reduced by annealing the silicon substrate and SiGe layer at 650-950°C in an inactive atmosphere for 30 seconds - 30 minutes, and a process where the layer of silicon applied with tensile strain is deposited on the reduced SiGe layer by a thickness of 50-30 nm.



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[Date of extinction of right]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] The process which is the manufacture approach of the semi-conductor substrate which includes the approach of forming the SiGe layer which has comparatively high germanium concentration, and offers a silicon substrate, the process from which germanium concentration deposits on the thickness of about 100nm - 500nm the SiGe layer which is 22% or more in a mole fraction, and about 1.1016 -- with the dose of cm-2-5.1016cm-2 In the process which injects H+ ion into this SiGe layer with the energy of abbreviation 20keV-40keV, and an inert atmosphere At the temperature of about 650 degrees C - 950 degrees C, heat annealing of this silicon substrate and this SiGe layer is carried out for [about 30 seconds -] 30 minutes. The manufacture approach of a semi-conductor substrate including the process which eases this SiGe layer, and the process which deposits the silicon layer which tensile strain required on this relaxation SiGe layer at the thickness of about 5nm - 30nm.
[Claim 2] The approach according to claim 1 the process which deposits the layer of said SiGe deposits the layer of this SiGe at the temperature of about 400 degrees C - 600 degrees C.
[Claim 3] The approach according to claim 1 of including further the process which deposits the layer of a silicon oxide on said SiGe layer before said impregnation process at the thickness of about 50A - 300A.
[Claim 4] The approach according to claim 1 of including further the process which deposits the layer of the relaxation SiGe which has the thickness of about 100nm on said relaxation SiGe layer after said heat annealing process.
[Claim 5] Said heat annealing process is an approach according to claim 1 performed in argon atmosphere.
[Claim 6] The process which offers the silicon substrate chosen from either of the substrates which are the manufacture approaches of the semi-conductor substrate which includes the approach of forming the SiGe layer which has comparatively high germanium concentration, and consist of bulk silicon and SIMOX, germanium concentration 25% or more of SiGe layer with a mole fraction at the temperature within the limits of about 400 degrees C - 600 degrees C the process deposited on the thickness of about 100nm - 500nm, and about 1.1016 -- with the dose of cm-2-5.1016cm-2 In the process which injects H+ ion into this SiGe layer with the energy of abbreviation 20keV-45keV, and argon atmosphere At the temperature of about 650 degrees C - 950 degrees C, heat annealing of this silicon substrate and this SiGe layer is carried out for [about 30 seconds -] 30 minutes. The manufacture approach of a semi-conductor substrate including the process which eases this SiGe layer, and the process which deposits the layer of the silicon which tensile strain required on this relaxation SiGe layer at the thickness of about 5nm - 30nm.
[Claim 7] The approach according to claim 6 of including further the process which deposits the layer of a silicon oxide on said SiGe layer before said impregnation process at the thickness of about 50A - 300A.
[Claim 8] The approach according to claim 6 of including further the process which deposits the layer of the relaxation SiGe which has the thickness of about 100nm on said relaxation SiGe layer after said heat annealing process when the thickness of said relaxation SiGe layer is less than 300nm.

[Claim 9] At the process which is the manufacture approach of the semi-conductor substrate which

includes the approach of forming the SiGe layer which has comparatively high germanium concentration, and offers a silicon substrate, and the temperature within the limits of about 400 degrees C - 600 degrees C the process from which germanium concentration deposits 22% or more of SiGe layer on the thickness of about 100nm - 500nm in a mole fraction, and about 1.1016 -- with the dose of cm-2-5.1016cm-2 In the process which injects H+ ion into this SiGe layer with the energy of abbreviation 20keV-45keV, and an inert atmosphere At the temperature of about 650 degrees C - 950 degrees C, heat annealing of this silicon substrate and this SiGe layer is carried out for [about 30 seconds -] 30 minutes. The manufacture approach of a semi-conductor substrate including the process which eases this SiGe layer so that at least 70% of relaxation may be attained, and the process which deposits the layer of the silicon which tensile strain required on this relaxation SiGe layer at the thickness of about 5nm - 30nm.

[Claim 10] The approach according to claim 9 of including further the process which deposits the layer of a silicon oxide on said SiGe layer before said impregnation process at the thickness of about 50A - 300A.

[Claim 11] Said heat annealing process is an approach according to claim 9 performed in argon atmosphere.

[Claim 12] The approach according to claim 9 of including further the process which deposits the layer of the relaxation SiGe which has the thickness of about 100nm on said relaxation SiGe layer after said heat annealing process.

[Claim 13] The approach according to claim 12 by which the process which deposits the layer of the relaxation SiGe which has the thickness of about 100nm on said relaxation SiGe layer only when the thickness of said relaxation SiGe layer is less than 300nm is performed.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] (Related application) This application relates to the United States patent application 09th for which it applied on April 3, 2000 / the "approach which forms a thick relaxation SiGe layer on Si" of No. 541,255, and the United States patent application 09th for which it applied on February 13, 2001 / the "approach of reducing the leakage current of Si1-xGexCMOS" of No. 783,817.
(Field of invention) This invention relates to the manufacture approach of the semi-conductor substrate which includes in a detail the process which forms a SiGe layer using hydrogen impregnation about the manufacture approach of semi-conductor substrates, such as a high-speed CMOS integrated circuit.
[0002]
[Description of the Prior Art] In the MOSFET device application whose mobility improved, in order to raise carrier mobility nMOS device (Welser and others) ["Strain] dependence of the performance enhancement in strained-Si n-MOSFETs" IEDM Conference Proceedings p. 373 (1994) (nonpatent literature 1) Rim's and others "Fabrication andanalysis of Deep submicron strained-Si N-MOSFETs" IEEE Transactions onElectron Devices Vol47 1406 (2000) (nonpatent literature 2) And Rim's and others "Strained Si NMOSFETs for high performance CMOS technology 2001 Symposium on VLSI Technology Digest of Technical Papers, IEEE p.59, 2001 (nonpatent literature 3), and pMOS device (Rim and others) ["Enhanced hole mobilities in surface-channel strained-Si] p-MOSFETs" IEDMConference Proceedings p.517 (nonpatent literature 4) (1995), And Nayak's and others "High-mobilityStrained-Si PMOSFETs" IEEE Transactions on Electron Devices Vol.43, 1709 (1996) (nonpatent literature 5) About both, the thick Si1-xGex buffer layer by which stress relaxation was carried out is used as a virtual substrate for a thin distorted silicon layer. As compared with the bulk silicon device, it is reported to the reference in 2001 of Rim and others in the device which is Leff<70nm that electron mobility improved 70%. High electric-field Hall mobility in a long channel device (it is reported by Nayak and others that high-field hole mobility improved to 40%.)
[0003] A thick Si1-xGex layer by formation of a misfit rearrangement plastically Distortion (stress) eases (R. Hull and others). ["Nucleation of misfit dislocations in strained-layer epitaxy in the GexSi1-x/Si] system" J. Vac Sci. Technol. A7 2580 1989 (nonpatent literature 6), "Strain relaxationkinetics in Si1-xGex/Si heterostructures" of Houghton J. Appl. Phys. 70 2136 1991 (nonpatent literature 7), Wickenhauser's and others "Determination of the activation energy for theheterogeneous nucleation of misfit dislocations in Si1-xGex/Si depositedby selective epitaxy" Appl. Phys.Lett. 70 324 1997 (nonpatent literature 8), Matthews's and others "Defects in epitaxialmultilayers" J. Cryst. Growth 27 118 1974 (nonpatent literature 9), And Tang's and others "Investigation of dislocations in Si1-xGex/Si heterostructures grown by LPCVD" J.Cryst. Growth 125 301 1992 (nonpatent literature 10).
[0004] However, a penetration rearrangement usually occurs between this process. The engine performance of a device falls by existence of a penetration rearrangement, and the yield of a device falls remarkably.
[0005] The current latest technique of manufacturing the strain relaxation Si1-xGex buffer layer of high quality the rate of a presentation is growth of the layer which has different (it inclined)

thickness of several micrometers in the thickness direction (the above-mentioned reference in 2000 by Rim and others --) Nayak's and others above-mentioned reference, Schaeffler's and others "High-electron-mobility Si/SiGe heterostructures: influence ofthe relaxed SiGe buffer layer" Semiconductor. Sci. Technol. 7.260 1992 (nonpatent literature 11), And Fitzgerald's and others "Totally relaxed GexSi 1-x layers with low threading dislocation densities grown onSi substrates" Appl. Phys. Lett., 59 811 1991 (nonpatent literature 12). However, the consistency of a penetration rearrangement still exceeds 10E6cm-2 highly, for example, typically. Furthermore, it is not realistic to include the Si1-xGex layer which has the thickness of several micrometers in manufacture of the device which can use commercial. Research is done also about relaxation of the SiGe growth on a SIMOX (Separation by Implantation of Oxygen) wafer, and a Si/SiGe double layer is served in this case as free floating foil (free-floating foil) evenly maintained by the substrate. However, the ratio of the thickness of silicon and a SiGe layer must be controlled by accuracy so that the nucleation of the rearrangement from a SiGe layer to a silicon layer and the skid of a rearrangement happen. Moreover, in order to enable it to use this technique for almost all technical applications, A lot of germanium It needs to be developed so that it may contain (). [LeGouse's and others "Relaxation of SiGe thin films grown - Si/SiO2 substrates",] [J. Appl.] Phys. 75 (11) 1994 (nonpatent literature 13), And Powell's and others "New approach to the growth of low dislocation relaxed SiGe material" Appl. Phys. Lett. vol.64 1856 (nonpatent literature 14) (1994).

[0006] It turns out that it has a short-distance mutual attracting action with the hole powerful between rearrangements formed in silicon, germanium, and those alloys of helium impregnation and annealing. By preparing a hole in a SiGe/Si interface, the rate of stress relaxation improves substantially and the rearrangement fine structure deforms. However, reduction of penetration dislocation density was not observed (Follstaedt's and others "Cavity-dislocation interactions in Si-germanium and implications for heterostructure relaxation", Appl. Phys. Lett., 69, 2059, 1996 (nonpatent literature 15)). In order to attain 80% of relaxation, it is necessary to still perform annealing at about 1000 degrees C for 1 hour.

[0007] Moreover, it turns out that exfoliation of silicon is caused by hydrogen impregnation and shearing of the detailed layer formed with silicon occurs by it (Weldon's and others "On the mechanism of the hydrogen-inducedexfoliation of silicon", J. Vac. Sci.Technol. B. 15, 1065, 1997 (nonpatent literature 16)). This technique is used for manufacture of a high quality SOI (silicon-on-insulator) wafer, and is well-known as a "SmartCut" (trademark) process. The latest reference (S. Mantl's and others reference and H.Trinkaus's and others reference) by joint research of Germany raised whenever [relaxation / of SiGe] using hydrogen impregnation, and has reported the advantage of reducing the consistency of a penetration rearrangement. It implantation(s). S. -- Mantl's and others "Strain relaxation of epitaxial SiGe layers - Si(100) improved by hydrogen [ ] -- Nuclear Instruments and Methods in Physics ResearchB 147 29 (1999) (nonpatent literature 17) And H.Trinkaus's and others "Strain relaxation mechanismfor hydrogen-implanted Si1-xGex/Si (100) heterostructures" Appl. Phys. Lett. 76 3552 2000 (nonpatent literature 18), however the above-mentioned researchers Thickness is only 2000A - 2500A, and relaxation of the SiGe layer whose germanium concentration is less than 22% in molar weight is reported. The SiGe layer which has such thickness is not enough for commercial device application. The approach of forming the thicker film is indicated by the United States patent application 09th which is related application / No. 541,255, and the method of reducing the leakage current by suitable insulation is indicated by the United States patent application 09th which is related application / No. 783,817. The related United States patent application 09th / No. 541,255 have indicated formation of the SiGe thin film containing about 21% of germanium. In order to increase the distortion in a cap silicon channel and to raise electron mobility and Hall mobility further, it is desirable to make germanium concentration higher.

[0008] In case joint research of Germany forms the SiGe layer containing germanium to 30% eased substantially It is reported that helium impregnation is effective (). [M.] Luysberg's and others "Relaxation of Si1-xGex bufferlayers on Si (100) through Helium implantation" Abstracts of the 2001 MRS Spring Meeting Abstract P5.4 April 18 2001 (nonpatent literature 19).

[0009]

[Nonpatent literature 1] Welser's and others "Strain dependence of the performance enhancement in

strained-Si n-MOSFETs" IEDM Conference Proceedings p.373 1994 [Nonpatent literature 2] Rim's and others "Fabrication and analysis of Deep submicron strained-Si N-MOSFETs" IEEE Transactions on Electron Devices Vol47 1406 2000 [nonpatent literature 3] Rim's and others "Strained Si NMOSFETs for highperformance CMOS technology 2001 Symposium on VLSI Technology Digest of Technical Papers p.59 IEEE 2001 [nonpatent literature 4] pMOS device (Rim's and others "Enhanced hole mobilities in surface-channel strained-Sip-MOSFETs", IEDM Conference Proceedings, p. 517, 1995, [nonpatent literature 5]) Nayak's and others "High-mobility Strained-Si PMOSFETs" IEEE Transactions on Electron Devices Vol.43 1709 (1996) [Nonpatent literature 6] R. Hull's and others "Nucleation of misfit dislocations in strained-layer epitaxy inthe GexSi1-x/Si system" J. Vac Sci. Technol. A7 2580 1989 [Nonpatent literature 7] "Strain relaxation kinetics in Si1-xGex/Si heterostructures" of Houghton, J. Appl. Phys. 70 2136 1991 [Nonpatent literature 8] Wickenhauser's and others "Determination of theactivation energy for the heterogeneous nucleation of misfit dislocations in Si1-xGex/Si deposited by selective epitaxy" Appl. Phys. Lett. 70 324 1997 [Nonpatent literature 9] Matthews's and others "Defects in epitaxial multilayers" J. Cryst. Growth 27 118 1974 [Nonpatent literature 10] Tang's and others "Investigation of dislocations in Si1-xGex/Si heterostructures grown by LPCVD" J. Cryst. Growth 125 301 1992 [nonpatent literature 11] Schaeffler's and others "High-electron-mobilitySi/SiGe heterostructures : influenceof the relaxed SiGe buffer layer", Semiconductor. Sci. Technol. 7.260 1992 [nonpatent literature 12] Fitzgerald's and others "Totally relaxed GexSi1-x layers with low threading dislocation densities grown - Si substrates" Appl. Phys. Lett. 59 811 1991 [nonpatent literature 13] LeGouse's and others "Relaxation of SiGe thin films grown - Si/SiO2 substrates" J. Appl. Phys. 75 (11) 1994 [nonpatent literature 14] Powell's and others "New approach to the growthof low dislocation relaxed SiGe material" Appl. Phys. Lett. vol. 64, 1856, 1994 [nonpatent literature 15] Follstaedt's and others "Cavity-dislocation interactions in Si-germanium and implicationsfor heterostructure relaxation", Appl. Phys. Lett. 69 2059 1996 [nonpatent literature 16] Weldon's and others "On the mechanism of the hydrogen-induced exfoliation of silicon", J. Vac. Sci. Technol. B. 15 1065 1997 [nonpatent literature 17] S. Mantl's and others "Strain relaxation of epitaxial SiGe layers on Si (100) improved by hydrogen implantation NuclearInstruments and Methods in Physics Research B 147 29 1999 [nonpatent literature 18] H. Trinkaus's and others "Strain relaxation mechanism for hydrogen-implanted Si1-xGex/Si(100) heterostructures" Appl. Phys. Lett. 76 3552 2000 [nonpatent literature 19] M. Luysberg's and others "Relaxation of Si1-xGex buffer layers - Si(100) through Helium implantation" Abstracts of the 2001 MRS Spring Meeting AbstractP 5.4 April 18 2001 [0010] [Problem(s) to be Solved by the Invention] In the oral announcement of this paper, 18keV helium ion is poured in with the dose of 1.1016cm-2-3.1016cm-2, and it is concretely reported in the SiGe layer with a thickness of 100nm which has 30% of germanium concentration to which 750 degrees C - 1000 degrees C RTA processing was performed that 80% of stress relaxation was attained. The presenter has described concretely that hydrogen impregnation is not effective, when germanium concentration is higher than 22%. In order to form a stress relaxation SiGe layer with a smooth thickness of 100nm - 500nm which has germanium concentration exceeding 22%, helium impregnation is required and it is reported that hydrogen impregnation is not effective.

[0011] The object of this invention is forming the thick (for example, 100nm - 500nm) smooth SiGe layer (film) by which stress relaxation's was carried out using hydrogen impregnation as a buffer layer for the silicone film which the tensile strain which have high germanium concentration (22% or more, mole fraction), and which are used for high-speed MOSFET application required.

[0012]

[Means for Solving the Problem] The process which the manufacture approach of the semi-conductor substrate of this invention is the manufacture approach of the semi-conductor substrate which includes the approach of forming the SiGe layer which has comparatively high germanium concentration, and offers a silicon substrate, the process from which germanium concentration deposits on the thickness of about 100nm - 500nm the SiGe layer which is 22% or more in a mole fraction, and about 1.1016 -- with the dose of cm-2-5.1016cm-2 In the process which injects H+ ion into this SiGe layer with the energy of abbreviation 20keV-40keV, and an inert atmosphere At the temperature of about 650 degrees C - 950 degrees C, heat annealing of this silicon substrate and this SiGe layer is carried out for [about 30 seconds -] 30 minutes, and the process which eases this SiGe

layer, and the process which deposits the silicon layer which tensile strain required on this relaxation SiGe layer at the thickness of about 5nm - 30nm are included.
[0013] The process which deposits the layer of said SiGe deposits the layer of this SiGe at the temperature of about 400 degrees C - 600 degrees C.
[0014] The process which deposits the layer of a silicon oxide on said SiGe layer before said impregnation process at the thickness of about 50A - 300A is included further.
[0015] The process which deposits the layer of the relaxation SiGe which has the thickness of about 100nm on said relaxation SiGe layer after said heat annealing process is included further.
[0016] Said heat annealing process is performed in argon atmosphere.
[0017] Moreover, the manufacture approach of the semi-conductor substrate of this invention is the manufacture approach of the semi-conductor substrate which includes the approach of forming the SiGe layer which has comparatively high germanium concentration. The process which offers the silicon substrate chosen from either of the substrates which consist of bulk silicon and SIMOX, and germanium concentration 25% or more of SiGe layer with molar weight at the temperature within the limits of about 400 degrees C - 600 degrees C the process deposited on the thickness of about 100nm - 500nm, and about 1.1016 -- with the dose of cm-2-5.1016cm-2 In the process which injects H+ ion into this SiGe layer with the energy of abbreviation 20keV-45keV, and argon atmosphere At the temperature of about 650 degrees C - 950 degrees C, heat annealing of this silicon substrate and this SiGe layer is carried out for [about 30 seconds -] 30 minutes, and the process which eases this SiGe layer, and the process which deposits the silicon layer which tensile strain required on this relaxation SiGe layer at the thickness of about 5nm - 30nm are included.
[0018] The process which deposits the layer of a silicon oxide on said SiGe layer before said impregnation process at the thickness of about 50A - 300A is included further.
[0019] When the thickness of said relaxation SiGe layer is less than 300nm, the process which deposits the layer of the relaxation SiGe which has the thickness of about 100nm on said relaxation SiGe layer after said heat annealing process is included further.
[0020] Moreover, the manufacture approach of the semi-conductor substrate of this invention is the manufacture approach of the semi-conductor substrate which includes the approach of forming the SiGe layer which has comparatively high germanium concentration, and they are the process which offers a silicon substrate, and the temperature within the limits of about 400 degrees C - 600 degrees C. the process from which germanium concentration deposits 22% or more of SiGe layer on the thickness of about 100nm - 500nm in a mole fraction, and about 1.1016 -- with the dose of cm-2-5.1016cm-2 In the process which injects H+ ion into this SiGe layer with the energy of abbreviation 20keV-45keV, and an inert atmosphere At the temperature of about 650 degrees C - 950 degrees C, heat annealing of this silicon substrate and this SiGe layer is carried out for [about 30 seconds -] 30 minutes. The process which eases this SiGe layer so that at least 70% of relaxation may be attained, and the process which deposits the layer of the silicon which tensile strain required on this relaxation SiGe layer at the thickness of about 5nm - 30nm are included.
[0021] The process which deposits the layer of a silicon oxide on said SiGe layer before said impregnation process at the thickness of about 50A - 300A is included further.
[0022] Said heat annealing process is performed in argon atmosphere.
[0023] The process which deposits the layer of the relaxation SiGe which has the thickness of about 100nm on said relaxation SiGe layer after said heat annealing process is included further.
[0024] Only when the thickness of said relaxation SiGe layer is less than 300nm, the process which deposits the layer of the relaxation SiGe which has the thickness of about 100nm on said relaxation SiGe layer is performed.
[0025] The above-mentioned object and above-mentioned summary of this invention are offered so that he can understand the essence of this invention quickly. By referring to detailed explanation of the suitable operation gestalt of this invention which relates with a drawing and is explained below, he can understand this invention more nearly thoroughly.
[0026]
[Embodiment of the Invention] Disclosure of this description shows that its hydrogen impregnation is dramatically useful in case the instruction by the conventional technique forms the SiGe film which has 22% or more of germanium concentration conversely and by which distortion (stress)

relaxation was carried out substantially. Although applied to the SiGe layer (film) which has germanium concentration which exceeds 22% for the technique of a publication by the molar weight ratio on these descriptions, when using the approach of this invention, the upper limit of germanium concentration is not directed. Although helium cannot passivate a defect, since it is known well that a defect can be passivated, in the case of commercial device application, hydrogen is more desirable [the hydrogen impregnation] than helium. using hydrogen impregnation, it has high germanium concentration (it is 22% or more at a mole fraction), and the approach of this invention has low penetration dislocation density -- the thick (for example, 100nm - 500nm) smooth SiGe layer (film) by which stress relaxation was carried out is formed.

[0027] The approach of this invention is first explained with reference to drawing 1 . Introduction and a silicon substrate 10 are offered. A silicon substrate 10 may be bulk silicon or SIMOX (Separation by Implantation of Oxygen). On a silicon substrate 10, the distorted SiGe layer 12 deposits at the thickness which is about 100-500nm. germanium concentration of the distorted SiGe layer 12 may be 22% or more by the atomic ratio (mole fraction). With the suitable operation gestalt of the approach of this invention, the SiGe layer 12 which has about 30% of germanium concentration is formed. Or the SiGe layer 12 to which inclined germanium profile, i.e., germanium concentration in the thickness direction, is so high that it becomes thick may be used. It is necessary to choose growth conditions and ingredient gas so that surface irregularity may be minimized, while securing good crystallinity. This means performing 400 degrees C - 600 degrees C low dental-curing length, and usually forming the metastable distorted SiGe film.

[0028] Reference of drawing 2 pours in H+ ion. The dose of H+ is within the limits of abbreviation 1.1016cm-2-5.1016cm-2. An energy level is usually within the limits of abbreviation 20keV-45keV, although it is dependent on the thickness of SiGe. In order to avoid contamination while an impregnation process is carried out, an about 50A - 300A (5-30nm) thin sacrifice silicon oxide layer (sacrificial silicon oxide layer) may be deposited on the SiGe layer 12.

[0029] Drawing 3 shows a heat annealing process. The distorted SiGe layer 12 changes with these heat annealing to the 1st distortion (stress) relaxation SiGe layer 14. Annealing is performed [in inert atmospheres, such as Ar,] over 30 minutes from about 30 seconds at the temperature within the limits of about 650 degrees C - 950 degrees C.

[0030] The 2nd SiGe layer 16 which consists of SiGe by which strain relaxation was carried out to arbitration is deposited on the relaxation SiGe layer 14 at the thickness of about 100nm or more if needed. The criteria the layer prepared in this arbitration judges it to be whether it is the need are the thickness of the relaxation SiGe layer 14. When the SiGe layer 14 is thinner than 300nm, it is required that the additional strain relaxation SiGe layer 16 should be formed so that the thickness of the final whole SiGe relaxation layer may be set to at least 300nm.

[0031] In the final process of the approach of this invention shown in drawing 5 , the silicon layer 18 which tensile stress required deposits on the relaxation SiGe layer 14 or the 2nd SiGe layer 16 so that it may have the thickness of about 5nm - 30nm.

[0032] Drawing 6 , drawing 7 and drawing 8 - drawing 10 show the condition after hydrogen impregnation of the SiGe film with a thickness of 200nm - 220nm which has about 25% - 30% of germanium concentration by the molar weight ratio, and thermal relaxation. germanium concentration is about 28 - 30%, and drawing 6 is drawing showing the Nomarski microscope image after performing hydrogen impregnation and thermal relaxation of the SiGe layer which has the thickness which is 200nm - 220nm. Drawing 7 is drawing showing the X diffraction of the SiGe layer shown in drawing 6 . Moreover, drawing showing a 400 times [after drawing 8 performs hydrogen impregnation of the SiGe film with a thickness of 300nm which has germanium profile with the dip where the presentation rate of the thickness direction changed, and annealing] as many Nomarski-microscope image as this, and drawing 9 are drawings showing a 1000 times [after performing hydrogen impregnation of the SiGe film with a thickness of 300nm which has germanium profile with dip, and annealing] as many Nomarski-microscope image as this. Drawing 10 is drawing showing the X diffraction of drawing 8 and the SiGe layer of drawing 9 .

[0033] Drawing 6 , drawing 8 , and the Nomarski microscope image of drawing 9 show the condition of a very flat front face. The reciprocal space map (reciprocal space map) of an X diffraction is shown, and, as for drawing 7 and drawing 10 , it is checked, respectively that strain

relaxation with the large crystal lattice from at least 70% to 85% is obtained from these maps. Reference of drawing 7 shows this condition of having been eased, by the offset between a silicon (224) peak and a SiGe (224) peak, as shown by the broken line.
[0034] Drawing 11 shows the Nomarski microscope image after performing hydrogen impregnation of the SiGe film which has the thickness of about 300nm which has germanium profile with dip, and annealing. Drawing 12 shows the X diffraction of the SiGe layer of drawing 11 . germanium concentration -- 21% to 30% of the SiGe layer front face on a silicon substrate -- almost -- linear -- changing . By using germanium profile with dip, the thickness of a SiGe layer can be increased easily and the SiGe layer which has a smooth front face and by which strain relaxation was carried out substantially can also be offered. The 2nd SiGe deposition usually has sufficient thickness are less thin, and, thereby, the quality of this SiGe layer of the whole SiGe layer improves.
[0035] All the SiGe layers that were constituted based on the approach of this invention and by which strain relaxation was carried out are used as a substrate for growing up the silicone film which tensile stress required. Then, nMOS which has the hole and electron mobility which improved, and a pMOS transistor are formed using these film. Drawing 6 and the SiGe thin film of drawing 7 have 28.6% of germanium concentration. a SiGe thin layer -- the thickness of about 200nm -- having -- the energy of about 25 keV(s) -- it is -- about 3.1016 -- with the ion dose of cm-2, H+ ion implantation is performed and it is formed. Annealing of the wafer is carried out for about 10 minutes at about 800 degrees C in the argon atmosphere in a RTA chamber. The 1000 times as many Nomarski microscope image as this shows the smoother front face. The reciprocal space map of the X diffraction of drawing 7 shows a big central peak. This peak is a silicon (-2-24) substrate peak. The peak of the smaller one which lasts to the right from the bottom is acquired from the SiGe layer eased selectively. From the relative location of these two peaks, a SiGe layer has **0.5% of germanium 28.2%, and stress is eased **3% 75.8%.
[0036] Drawing 8 , drawing 9 , and drawing 10 show the 1st smooth (for example, about 85%) SiGe layer which has about 30% of germanium concentration and by which stress relaxation was carried out substantially. The thickness whose example of this is about 30% and whose germanium concentration in a SiGe layer is a SiGe layer is about 220nm. SiO2 about 20nm cap is formed of PECVD. H+ ion implantation -- the energy of about 26 keV(s) -- it is -- about 3.1016 -- it is carried out with the ion dose of cm-2. Annealing of the wafer is carried out for 9 minutes at about 800 degrees C in the argon atmosphere in a RTA chamber. Drawing 9 shows the 400 times as many Nomarski microscope image photoed in the center of a wafer as this. Drawing 9 is the 1000 times as many NOMARU skiing image similarly photoed in the center of a wafer as the same wafer. Drawing 10 shows the X diffraction of the wafer, the SiGe film has **0.5% of germanium concentration 29.7%, and stress relaxation is carried out **3% 85.2%.
[0037] Drawing 11 and drawing 12 show the dip germanium sample which was eased substantially and which has a smooth front face. Drawing 11 is the smooth (for example, about 82%) Nomarski microscope image of the 1st SiGe layer eased substantially, and photos the core of a wafer by about 1000 times. Drawing 12 is drawing showing the X diffraction of the wafer of drawing 11 . The thickness of a SiGe layer is about 301nm, and has about 21% - 30% of germanium dip profile in the condition [having made it grow up freely]. H+ ion implantation -- the energy level of about 32 keV (s) -- it is -- about 2.1016 -- it is carried out with the ion dose of cm-2. Annealing of the wafer is carried out for 9 minutes at about 800 degrees C in the argon atmosphere in a RTA chamber. A SiGe layer has **0.5% of germanium concentration 27.8%, and stress is eased **3% 82.2%.
(Other operation gestalten) The approach of this invention grow up the SiGe layer of the thickness exceeding 300nm, perform hydrogen impregnation (H-II), perform RTA (make the stress of a SiGe layer ease), and may be change by form a **** EPISHI recon cap / channel by it so that a dip germanium profile may have bigger germanium concentration than 22% in the front face of a layer. This operation gestalt does not need deposition of the 2nd SiGe layer.
[0038] Other operation gestalten of the approach of this invention grow up the 1st SiGe layer which has germanium profile which fixed germanium profile or dip attached. Perform hydrogen impregnation (H-II) and RTA is performed (making the stress of a SiGe layer ease). The 2nd SiGe layer which has germanium profile which fixed germanium profile with bigger germanium concentration in a front face than 22% or dip attached is grown up, and it includes forming a ****

EPISHI recon cap / channel by it. The sum total of the thickness of the SiGe layer of this operation gestalt of the approach of this invention needs to be 300nm or more.
[0039] As mentioned above, the approach of forming the relaxation SiGe layer which has high germanium concentration was indicated. It is understood that the further deformation and the further correction can be made within the limits of this invention specified to the claim.
[0040]
[Effect of the Invention] as for the manufacture approach of the semi-conductor substrate of this invention, a mole fraction has 22% or more of high germanium concentration in this way using hydrogen impregnation -- the thick smooth SiGe layer by which stress relaxation was carried out can be formed, and a high speed MOSFET can be manufactured by the SiGe layer.

[Translation done.]

* NOTICES *

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is drawing showing the SiGe deposition approach of this invention.
[Drawing 2] It is drawing showing the SiGe deposition approach of this invention.
[Drawing 3] It is drawing showing the SiGe deposition approach of this invention.
[Drawing 4] It is drawing showing the SiGe deposition approach of this invention.
[Drawing 5] It is drawing showing the SiGe deposition approach of this invention.
[Drawing 6] It is drawing showing the Nomarski microscope image after performing hydrogen impregnation and thermal relaxation of the SiGe film which has the thickness germanium concentration is about 28 - 30%, and is [thickness] 200nm - 220nm.
[Drawing 7] It is drawing showing the X diffraction of the wafer of drawing 6 .
[Drawing 8] It is drawing showing a 400 times [after performing hydrogen impregnation of the SiGe film with a thickness of 300nm which has germanium profile with dip, and annealing] as many Nomarski microscope image as this.
[Drawing 9] It is drawing showing a 1000 times [after performing hydrogen impregnation of the SiGe film with a thickness of 300nm which has germanium profile with dip, and annealing] as many Nomarski microscope image as this.
[Drawing 10] It is drawing showing the X diffraction of drawing 8 and the SiGe layer of drawing 9 .
[Drawing 11] It is drawing showing the Nomarski microscope image of a SiGe layer with a thickness of 300nm formed so that it might have a profile with dip.
[Drawing 12] It is drawing showing a 1000 times as many X diffraction as the SiGe layer which has the thickness of 300nm of drawing 11 .
[Description of Notations]
10 Silicon Substrate
12 Distorted SiGe Layer
14 Relaxation SiGe Layer
16 2nd SiGe Layer
18 Silicon Layer

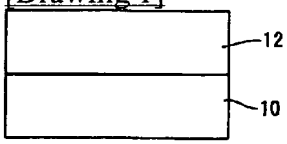
[Translation done.]

* NOTICES *

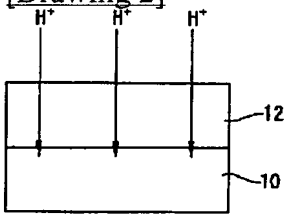
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

[Drawing 1]



[Drawing 2]



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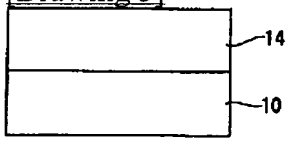
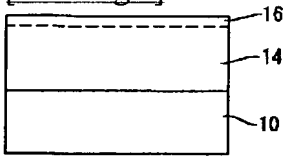


[Drawing 4]



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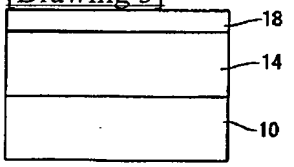

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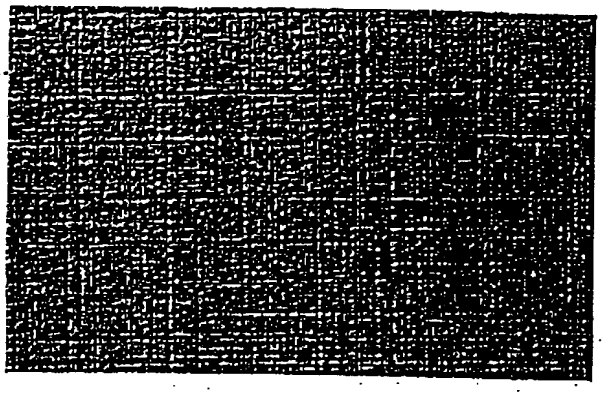
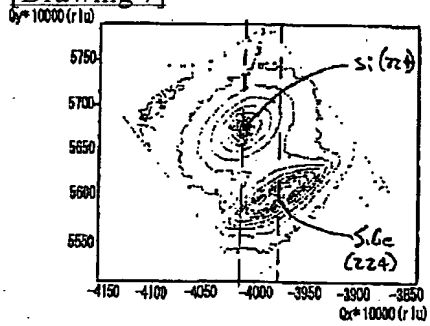
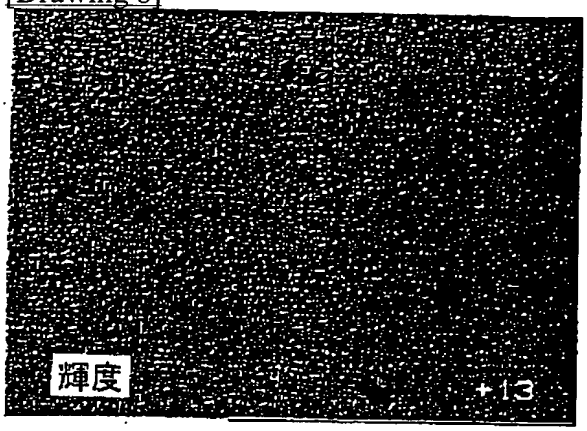


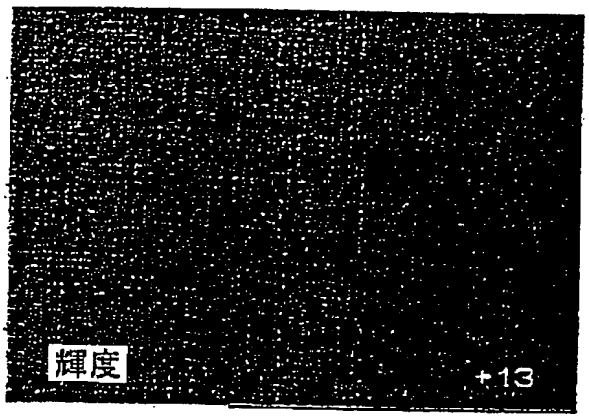
[Drawing 7]



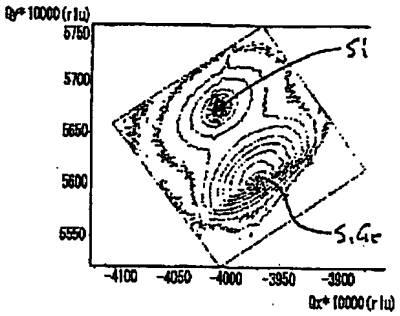
[Drawing 8]



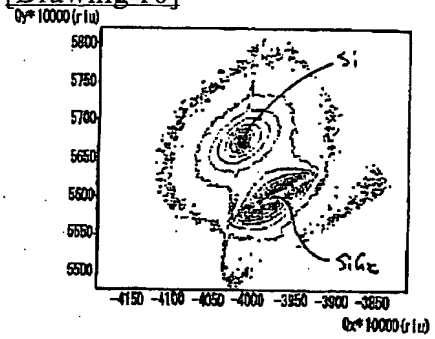
[Drawing 9]



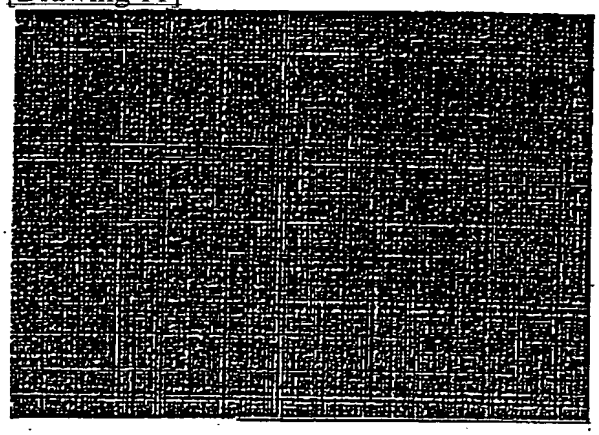
[Drawing 12]



[Drawing 10]



[Drawing 11]



[Translation done.]